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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/719,193	11/21/2003	Thaddeus John Gabara	91-2-36	2999

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EXAMINER	
HOLLINGTON, JERMELE M	
ART UNIT	**PAPER NUMBER**
2829	

DATE MAILED: 07/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/719,193	GABARA ET AL.	
	Examiner	Art Unit	
	Jermele M. Hollington	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,4,6-8,10-13 and 18-20* is/are rejected.

7)☒ Claim(s) *2,5,9 and 14-16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. Claims 1, 3-4, 6-8, 10-13, and 18-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Whetsel (5969538) in view of admitted prior art of Fig. 2.

Regarding claim 1, Whetsel discloses an apparatus comprising an integrated circuit die (not number but see Figs. 5, 7A-11B and 13A-14B) and comprising a signal pad (input pad D-1) arranged at a location of the die, a peripheral signal pad (output pad B-1) arranged proximate the periphery of the die, and a switch (switch 71, 77 or 79) coupled between the signal pad (D-1) and the peripheral signal pad (B-1); the switch (71, 77 or 79) being configurable in at least a first state (see Fig. 7B with switches 77 and 79 closed and switch 71 open) in which the signal pad (D-1) is not operatively connected to the peripheral signal pad (B-1), and a second state (see Fig.

7A with switch 71 closed and switches 77 and 79 open) in which the signal pad (D-1) is operatively connected to the peripheral signal pad (B-1); the switch (71, 77 or 79) being configurable in one of the first and second states responsive to a control signal having one of first and second signal characteristics, respectively; wherein the switch (77 and 79) is configured in the first state during normal operation of the integrated circuit die; and wherein the switch (71) is configured in the second state to permit test access to the signal pad (D-1) via the peripheral signal pad (B-1). However, he does not disclose an internal signal pad as claimed. The admitted prior art disclose an apparatus comprising an integrated circuit die (100') comprising an internal signal pad (internal signal pad 106) arranged at a location away from a periphery of the die (100'), a peripheral signal pad (signal pad 102) arranged proximate the periphery of the die (100'). Further, admitted prior art of Fig. 2 teaches that the addition of internal signal pad is advantageous because this placement allows many more buffer circuits to be placed on a single integrated circuit die than the simple outer perimeter placement of a regular die. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the apparatus of Whetsel by adding an internal signal pad as taught by the admitted prior art in order to allowed many more buffer circuits to be placed on a single integrated circuit die than the simple outer perimeter placement of a regular die.

Regarding claim 3, Whetsel discloses at least one of the signal pads (D-1) and the peripheral signal pad (B-1) has a buffer circuit (ISH circuit) associated therewith.

Regarding claim 4, Whetsel discloses the signal pad (D-1) is part of an area array of the integrated circuit die (see Fig. 5).

Regarding claim 6, Whetsel discloses the switch (71) is arranged nearer to the signal pad (D-1) than to the peripheral signal pad (B-1).

Regarding claim 7, Whetsel discloses the switch (71) is arranged immediately adjacent to the signal pad (D-1), so as to minimize parasitic elements associated with the signal pad (D-1) when the switch (71) is in the first state.

Regarding claim 8, Whetsel discloses the test access to the signal pad (D-1) via the peripheral signal pad (B-1) involves establishing electrical contact between an external probe [se Fig. 4] and the peripheral signal pad (B-1).

Regarding claim 10, Whetsel discloses the switch (71) is configured in the second state in conjunction with wafer-level testing of the integrated circuit die prior to separation of the die from a corresponding semiconductor wafer (shown in Fig. 3B).

Regarding claim 11, Whetsel discloses the integrated circuit die further comprises a control circuit (tester in Fig. 4) configured to generate the control signal for controlling the state of the switch (71, 77 and 79).

Regarding claim 12, Whetsel discloses the control signal (via tester of Fig. 4) having one of the first and second signal characteristics comprises the control signal being at one of a first signal level and a second signal level, respectively.

Regarding claim 13, Whetsel discloses the control circuit (tester 4) comprises at least one inverter (I), an output of the inverter (I) being coupled to a control signal input of the switch (71).

Regarding claim 18, Whetsel discloses the integrated circuit die is part of a semiconductor wafer (not number but shown in Fig. 3B) containing a plurality of dies (1-57).

Regarding claim 19, Whetsel discloses a method of providing access to a signal pad (input pad D-1) of an integrated circuit die (shown in Fig. 5), the signal pad (D-1) being arranged at a location away from a periphery of the die, the integrated circuit die further comprising a peripheral signal pad (output pad B-1) arranged proximate the periphery of the die and a switch (switch 71, 77 or 79) coupled between the signal pad (D-1) and the peripheral signal pad (B-1), the switch (71, 77 or 79) being configurable in at least a first state (see Fig. 7B) in which the signal pad (D-1) is not operatively connected to the peripheral signal pad (B-1), and a second state (see Fig. 7A) in which the signal pad (D-1) is operatively connected to the peripheral signal pad (B-1), the switch (71, 77 or 79) being configurable in one of the first and second states responsive to a control signal having one of respective first and second signal characteristics, the method comprising the steps of: configuring the switch (71, 77 or79) in the first state during normal operation of the integrated circuit die; and configuring the switch (71, 77 or 79) in the second state to permit test access to the signal pad (D-1) via the peripheral signal pad (B-1).

4. Claims 17 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Whetsel (5969538) in view of the admitted prior art of Fig. 2 above, and further in view of Fredrickson (6681352).

Regarding claim 17, Whetsel disclose an apparatus comprising an integrated circuit die (not number but see Figs. 5, 7A-11B and 13A-14B) and comprising a signal pad (input pad D-1) arranged at a location away from a periphery of the die, a peripheral signal pad (output pad B-1) arranged proximate the periphery of the die, and a switch (switch 71, 77 or 79) coupled between the signal pad (D-1) and the peripheral signal pad (B-1). However he does not disclose the integrated circuit die is packaged as claimed. Fredrickson discloses [see Fig. 2a] the integrated

circuit die (semiconductor die 110) is packaged within packaged integrated circuit (IC package 200). Further, Fredrickson teach that the addition of die in the IC package is advantageous because it provides that the die is a functional die and the package is used to by customers for varies testing function. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the apparatus of Whetsel by adding the die into a package as taught by Fredrickson in order to provide a functional die to be sent to customers for varies testing purposes.

Regarding claim 20, Whetsel discloses an apparatus comprising an integrated circuit die (not number but see Figs. 5, 7A-11B and 13A-14B) and comprising a signal pad (input pad D-1) arranged at a location away from a periphery of the die, a peripheral signal pad (output pad B-1) arranged proximate the periphery of the die, and a switch (switch 71, 77 or 79) coupled between the signal pad (D-1) and the peripheral signal pad (B-1); the switch (71, 77 or 79) being configurable in at least a first state (see Fig. 7B with switches 77 and 79 closed and switch 71 open) in which the signal pad (D-1) is not operatively connected to the peripheral signal pad (B-1), and a second state (see Fig. 7A with switch 71 closed and switches 77 and 79 open) in which the signal pad (D-1) is operatively connected to the peripheral signal pad (B-1); the switch (71, 77 or 79) being configurable in one of the first and second states responsive to a control signal having one of first and second signal characteristics, respectively; wherein the switch (77 and 79) is configured in the first state during normal operation of the integrated circuit die; and wherein the switch (71) is configured in the second state to permit test access to the signal pad (D-1) via the peripheral signal pad (B-1). However, he does not disclose a package integrated circuit with a lead frame coupled to the die as claimed. Fredrickson disclose [see Fig. 2A] a packaged

integrated circuit (IC package 200) comprising an integrated circuit die (semiconductor die 110); a lead frame (metal leads 220) coupled to the die (110); the integrated circuit die (110) and lead frame (220) being at least partially enclosed by a packaging material (package body 210). Further, Fredrickson teach that the addition of die in the IC package is advantageous because it provides that the die is a functional die and the package is used to by customers for varies testing function. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the apparatus of Whetsel by adding the die into a package as taught by Fredrickson in order to provide a functional die to be sent to customers for varies testing purposes.

Conclusion

5. Applicant's arguments with respect to claims 1-20 have been considered but are moot in view of the new ground(s) of rejection.

Allowable Subject Matter

6. Claims 2, 5, 9 and14-16 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

7. The following is a statement of reasons for the indication of allowable subject matter: regarding claim 2, the primary reason for the allowance of the claim is due to an apparatus comprising at least one of a internal signal pad and a peripheral signal pad comprises a bonding pad.

Regarding claim 5, the primary reason for the allowance of the claim is due to an apparatus comprising the internal signal pad comprises an analog signal pad.

Regarding claim 9, the primary reason for the allowance of the claim is due to an apparatus comprising an external probe comprises a test probe of a wire-typed wafer probe card.

Regarding claim 14, the primary reason for the allowance of the claim is due to an apparatus comprising a control circuit comprises first and second inverters connected in series, an output of the second inverters being coupled to a control signal input of the switch.

Regarding claim 15, the primary reason for the allowance of the claim is due to an apparatus comprising an input inverter is coupled via at least one resistor to a supply voltage terminal of the integrated circuit die.

Regarding claim 16, the primary reason for the allowance of the claim is due to an apparatus comprising an input of the inverter is coupled to an additional peripheral signal pad of the integrated circuit.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jermele M. Hollington whose telephone number is (571) 272-1960. The examiner can normally be reached on M-F (9:00-4:30 EST) First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nestor Ramirez can be reached on (517) 272-2034. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jermele M. Hollington
Primary Examiner
Art Unit 2829

JMH
July 22, 2005